Understanding Error Checking Using Parity Bytes in SDH/SONET Networks

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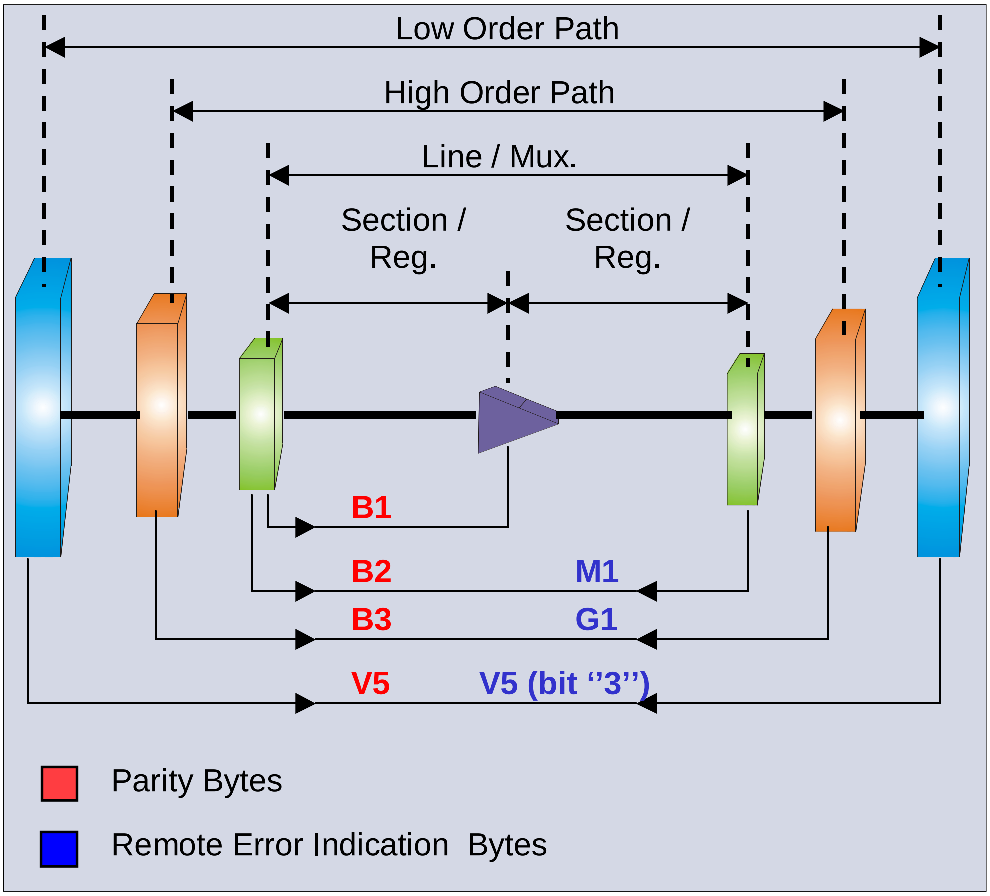
Compared to PDH/T-Carrier systems, SDH/SONET systems provide advanced network management features. One of the most important is that any bit errors can be assigned to a particular portion of the network, meaning that it is easier to isolate the source of the error.
This feature is made possible thanks to a special technique known as "Bit Interleaved Parity" (BIP).
The results of the BIP check for each link section of the network are inserted into parity bytes known as: B1, B2, B3, V5.



The BIP calculation method introduces some limitations. The limitations regarding the maximum error rates for B1, B2, B3, V5 bytes in SDH/SONET transmission system can be confusing.
The purpose of this application note is to provide some explanations about the BIP calculation method and the ensuing limitations.

1.0 Introduction

1.1 BIP: Definition

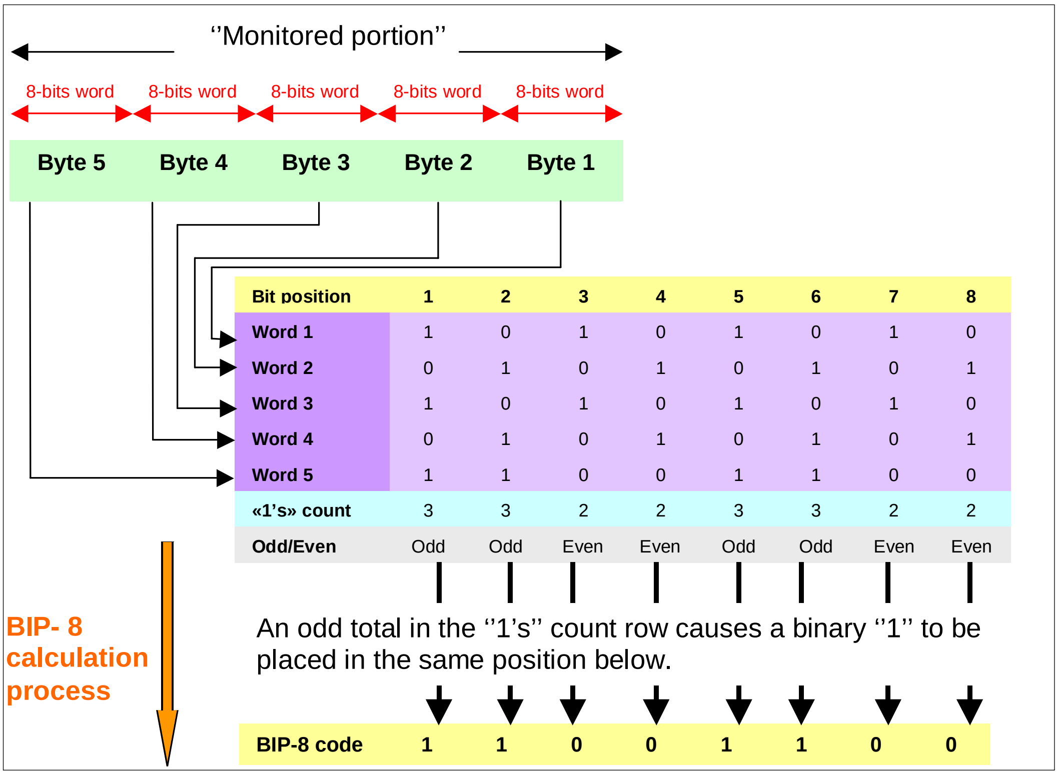
Bit Interleaved Parity (BIP-X) code is defined as a method of error monitoring. With “even” parity (as opposed to “odd” parity) an X-bit code is generated by the transmitting equipment over a specified portion (also called “block”) of the frame.
The BIP-X calculation principle is the following:
The monitored portion is divided in words of X-bit length. “X” can take the values: 1, 2, 8, 24, 96, etc...
The first bit of the BIP code provides even parity over the first bit of all the X-bit words in the portion of the frame in question, the second bit provides even parity over the second bit of all the X-bit words within the specified portion, etc...

Even parity is generated by setting the BIP-X bits, so that there is an even number of “1’s” in each monitored partition of the frame. A monitored partition comprises all bits which are in the same relative bit position within the X-bit words in the portion of the frame in question.

The example in the next paragraph illustrates this definition.

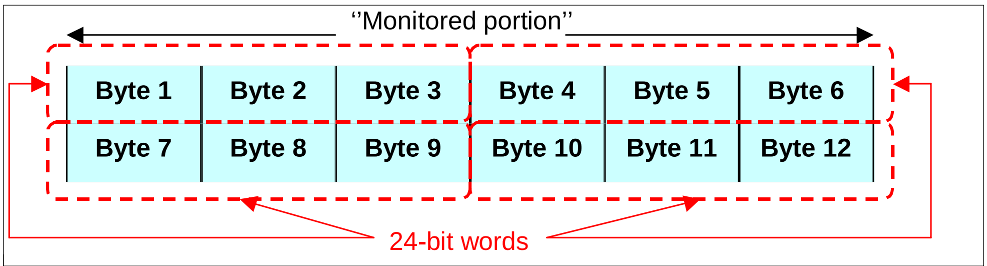
1.2 BIP: Examples of Calculations

The following example illustrates the calculation of a BIP-8 (X=8) over a “monitored portion” of 5 bytes:



Bit position	1	2	3	4	5	6	7	8
Word 1	1	0	1	0	1	0	1	0
Word 2	0	1	0	1	0	1	0	1
Word 3	1	0	1	0	1	0	1	0
Word 4	0	1	0	1	0	1	0	1
Word 5	1	1	0	0	1	1	0	0
«1’s» count	3	3	2	2	3	3	2	2
Odd/Even	Odd	Odd	Even	Even	Odd	Odd	Even	Even
BIP-8 code	1	1	0	0	1	1	0	0

A second example illustrates a BIP-24 calculation over a “monitored portion” of 12 bytes:



Bit position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Bytes 1-2-3	1	0	0	1	1	0	0	1	1	1	0	1	1	0	0	1	1	0	0	1	1	0	0	1
Bytes 4-5-6	0	1	1	1	0	1	0	0	0	0	1	1	1	0	1	0	1	1	0	0	1	1	1	1
Bytes 7-8-9	1	0	1	0	1	0	1	0	1	1	0	0	0	1	1	0	1	0	0	1	1	1	0	0
Bytes 10-11-12	0	1	0	1	0	1	0	1	0	1	1	0	0	0	1	1	1	0	0	1	1	0	0	1
"1's" count	2	2	2	3	2	2	1	2	2	3	2	2	2	1	3	2	4	1	0	3	4	2	1	3
Odd/Even	E	E	E	O	E	E	O	E	E	O	E	E	E	O	O	E	E	O	E	O	E	E	O	O
BIP-24 Code	0	0	0	1	0	0	1	0	0	1	0	0	0	1	1	0	0	1	0	1	0	0	1	1

1.3 Difference between "BIP-X" and "X BIP-1"

A BIP code can be exploited as a "BIP-X" and "X BIP-1". The calculation of "BIP-X" and "X BIP-1" is identical but the interpretation differs.

The concept of "Block" is fundamental to understanding the difference. In both cases, the size and the number of monitored blocks are different. This affects the number of errored blocks that can be detected and consequently affects the maximum error rate if the rates are displayed in "Equivalent BER" (very usual with SDH/SONET testers).

> **"Equiv BER"=(Number of errored blocks/sec) / (Total Number of bits/sec)**

If we take the BIP-8 example given in the previous paragraph and imagine that the line rate of the 5 bytes is 10 Mbit/s, then the differences between the 2 methods of calculation are shown below:

Monitored block

Byte 1	1	0	1	0	1	0	1	0
Byte 2	0	1	0	1	0	1	0	1
Byte 3	1	0	1	0	1	0	1	0
Byte 4	0	1	0	1	0	1	0	1
Byte 5	1	1	0	0	1	1	0	0
BIP-8 code	**1**	**1**	**0**	**0**	**1**	**1**	**0**	**0**

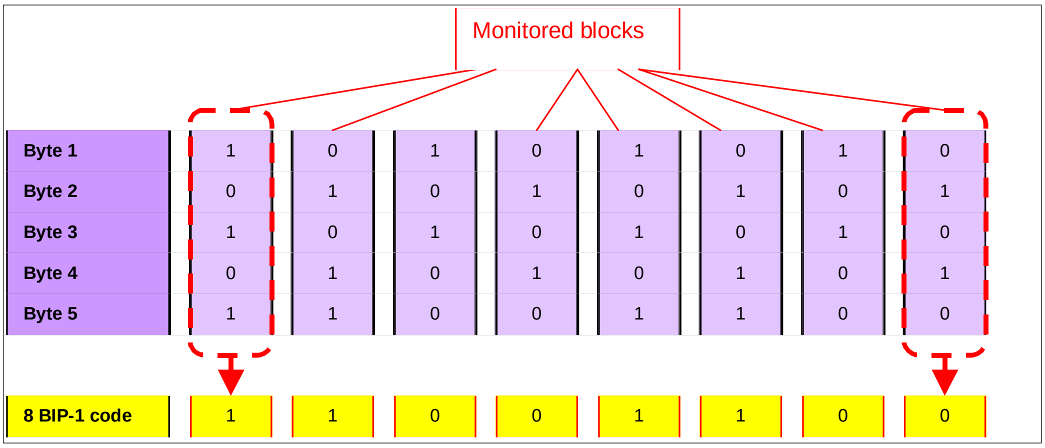
BIP-8

Size of the monitored block: 5 bytes (40 bits)

Number of blocks/sec: 250000

Max BER= (Maximum number of errored blocks/sec) / (Total number of bits/sec)

Max BER= 250000/10000000= 2.5 10^{-2}



8 BIP-1

Size of the monitored blocks: 5 bits
Number of blocks/sec: 2000000
Max BER= (Maximum number of errored blocks/sec) / (Total number of bits/sec)
Max BER= 2000000/10000000= $2\ 10^{-1}$

In conclusion, the maximum equivalent BER is “X” times higher with “X BIP 1” interpretation compared to “BIP-X” interpretation.

2.0 BIP Calculation applied to SDH/SONET Networks

As mentioned previously, the BIP technique allows error performance monitoring in real time in the SDH/SONET networks and is calculated on a frame by frame basis. The results of the BIP check for each link section of the network are inserted into parity bytes known as: B1, B2, B3, V5.
In addition, Remote Error Indication (REI) signals are sent back to the equipment at the originating end of a path.

2.1 “Block” Concept

The function of the SDH/SONET parity bytes (B1, B2, B3, V5) is more easily understood if they are associated with the definition of the “Block”:
“a set of consecutive bits associated with the path or the section; each bit belongs to one and only one block; consecutive bits may not be contiguous in time”.

In concrete terms, the table hereafter shows the “block” monitored by each parity byte:

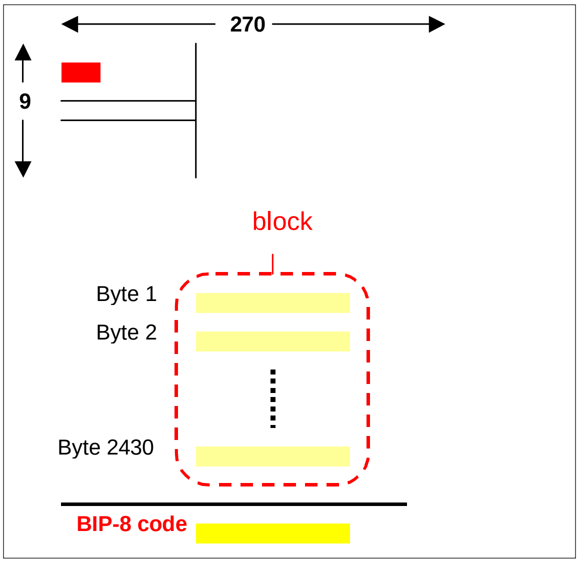
Parity Byte	Monitored ''Block''
B1	STM-n / OC-n B1
B2	STM-n / OC-n B2
B3	STM-n / OC-n B3
V5	VC-12 V5 140 bytes /500 µs VT-1.5 envelope capacity V5 104 bytes /500 µs

2.2 Parity Bytes: Definition

Parity Byte: B1

B1 byte is calculated over all bits of the previous STM-n/OC-n frame after it has been scrambled. This calculated value of B1 is then placed in the following frame before it is scrambled. B1 is a BIP-8(1).

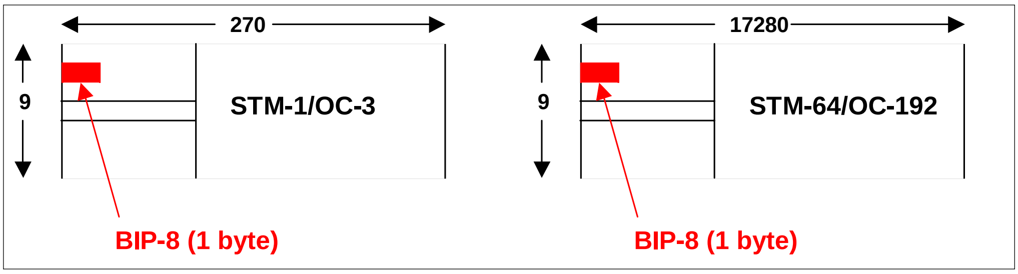
In the case of an STM-1/OC-3 frame, the value of the parity byte (B1) is calculated over 9 rows by 270 columns (or 2430 bytes). This represents 19440 bits which are protected by 8 parity bits:



Although the parity is calculated over the entire STM-n/OC-n frame, the number of parity bits remains the same when the size of the frame increases:

Notes:

[1] A recommendation, G.829, defined B1 as a "N.BIP-8" (for an STM-N frame). But it is only applicable for Hertzian and satellite transmission systems. This recommendation is not covered by this application note.



The table below summarizes the B1 parity byte characteristics according to the line rates:

Path	Bit Rate Kbit/s	Bit/block	Block/frame	Block/sec	B1[1]
STM0-Reg STS1-Sect	51840	6480	1	8000	BIP-8
STM1-Reg OC-3-Sect	155520	19440	1	8000	BIP-8
STM4-Reg OC-12-Sect	622080	77760	1	8000	BIP-8
STM16-Reg OC-48-Sect	2488320	311040	1	8000	BIP-8
STM64-Reg OC-192-Sect	9953280	1244160	1	8000	BIP-8

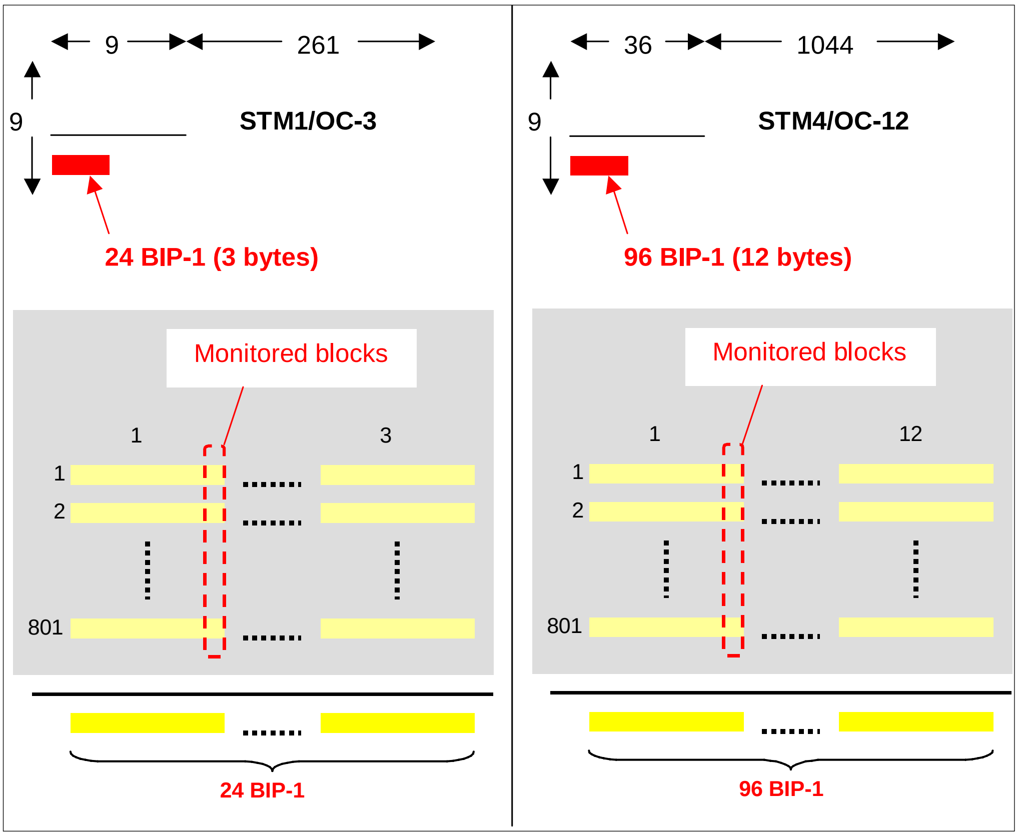
Notes:

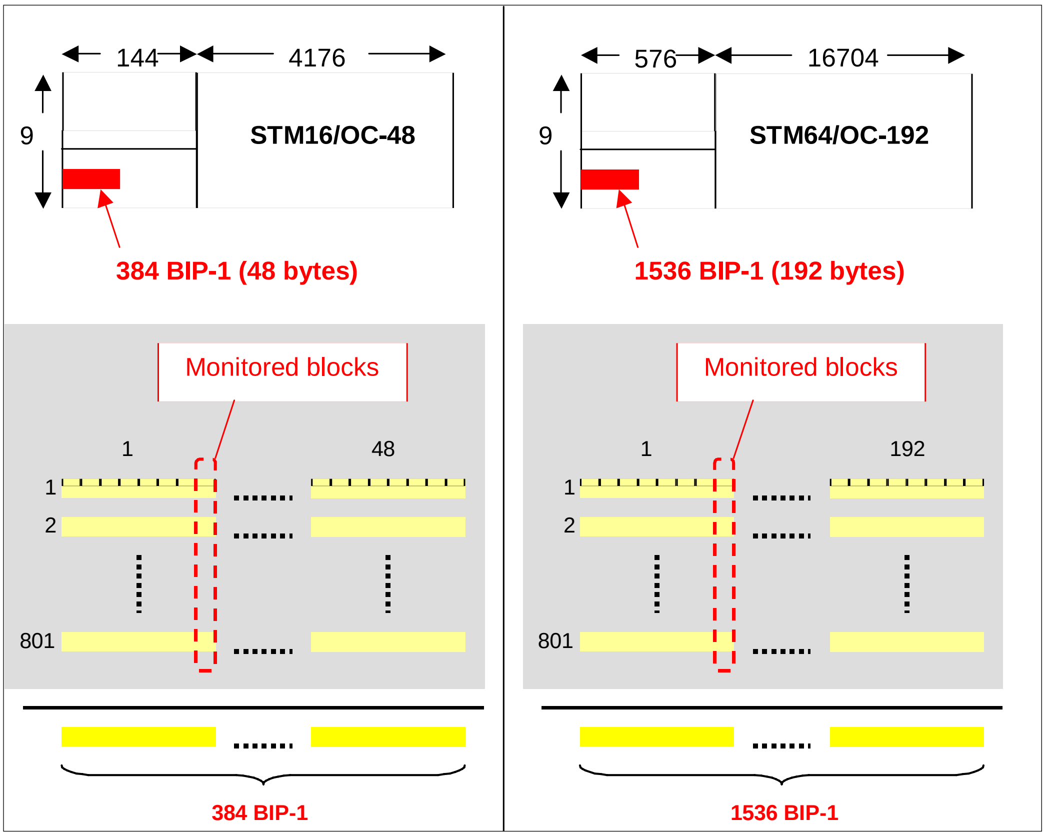
[1] Officially, there is no B1 definition for STM64/OC-192 frames. But it is widely accepted that the general B1 calculation method also applies to these frames.

[2] With "n" depending on the SDH/SONET frame.

Parity Byte: B2

B2 bytes are calculated prior to scrambling, but exclude the Regenerator/Section overhead bytes (A1, A2, J0, B1, E1, D1, D2, D3, etc...). The B2 bytes are then placed in the appropriate column, i.e B2 Col.1, B2 Col.2, B2 Col.3 (for an STM1/OC-3) of the following frame before it is scrambled. B2 is a n x 24 BIP-1[(2)].
This means that the number of parity bytes depends on the size of the frame, as shown below:





The table below summarizes the B2 parity bytes characteristics according to the line rates:

Path	Bit Rate Kbit/s	Bit/block	Block/frame	Block/sec	B2
STM0-Mux STS1-Line	51264	801	8	64000	8*BIP-1
STM1-Mux OC-3-Line	153792	801	24	192000	24*BIP-1
STM4-Mux OC-12-Line	615168	801	96	768000	96*BIP-1
STM16-Mux OC-48-Line	2460672	801	384	3072000	384*BIP-1
STM64-Mux OC-192-Line	9842688	801	1536	12288000	1536*BIP-1

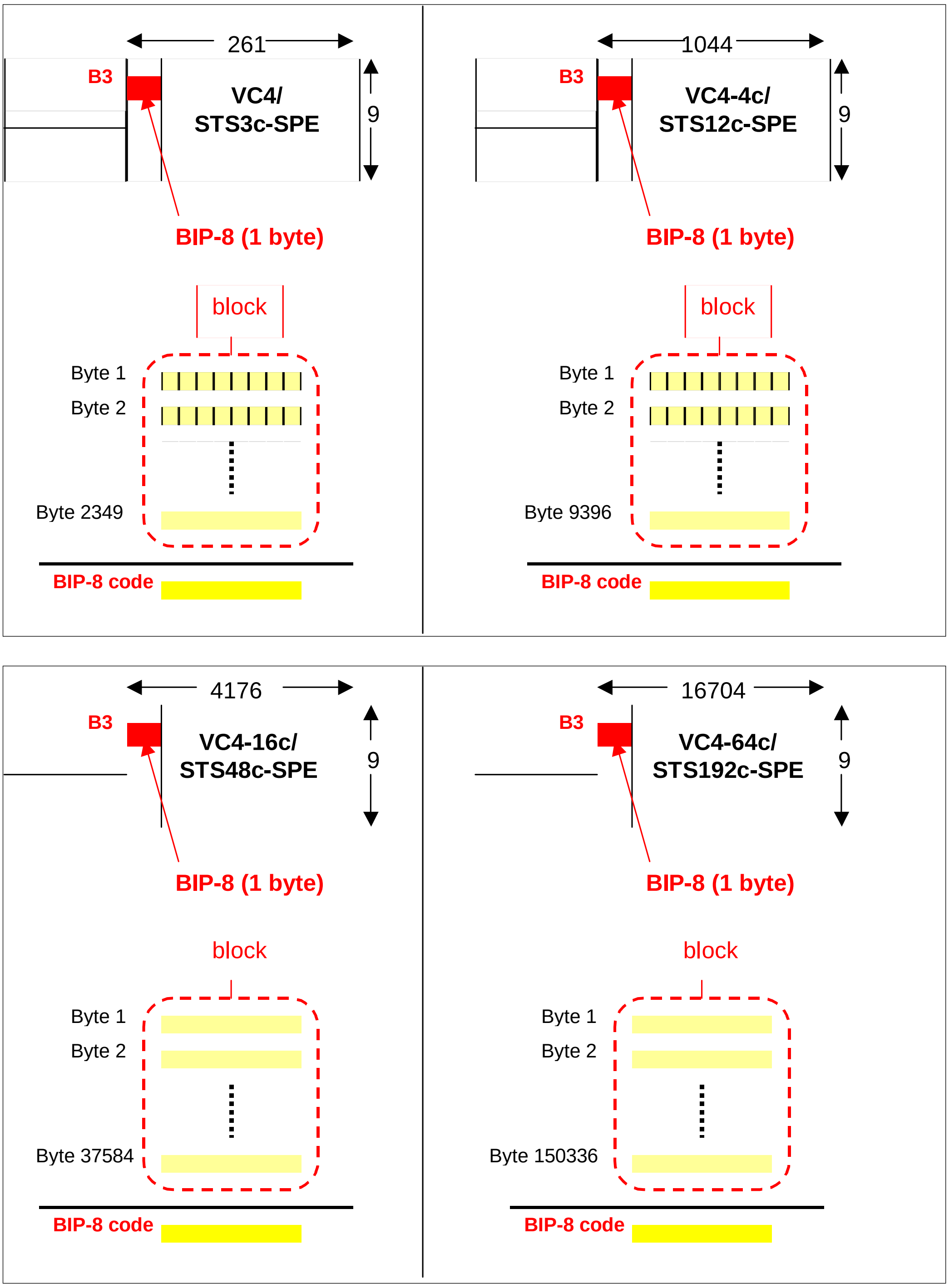
Parity Byte: B3

B3 is a BIP-8. B3 specifically does not include the SOH/TOH portion of the frame in its calculation which is made prior to scrambling. The result of the B3 calculation is placed in the following frame for each VC4/STS3-SPE.

The result that can be conveyed using the B3 depends directly on the type of mapping used (concatenated payload for example: VC4-4c, STS12c...).

For example, if VC4/STS-3c-SPE is used, then the number of bytes is given by 261 columns by 9 rows, or 2349 bytes. The number of bits protected by B3 is 18792.

Although the B3 parity is calculated over the different Virtual Containers (VC) or Synchronous Payload Envelopes (SPE), the number of parity bits remains the same when the size of the VC/SPEs increases (concatenated payload):



The table below summarizes the B3 parity byte characteristics according to the VC/SPEs:

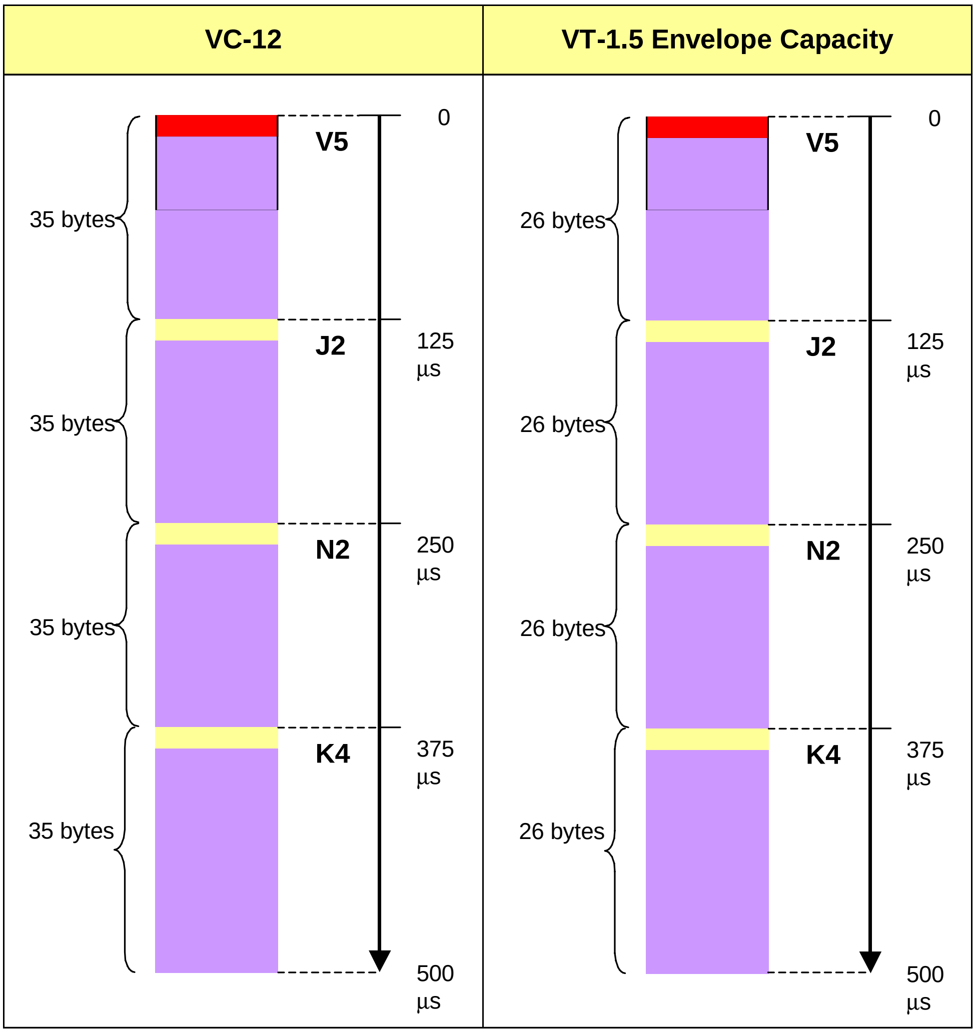
Path	Bit Rate Kbit/s	Bit/block	Block/frame	Block/sec	B3
VC3 STS 1-SPE	50112	6264	1	8000	BIP-8
VC4 STS 3c-SPE	150336	18792	1	8000	BIP-8
VC4-4c STS 12c-SPE	601344	75168	1	8000	BIP-8
VC4-16c STS 48c-SPE	2405376	300672	1	8000	BIP-8
VC4-64c STS 192c-SPE	9621504	1202688	1	8000	BIP-8

Parity Byte: V5

V5 is a BIP-2. Only 2 bits of the V5 byte are used to carry the BIP-2 result:

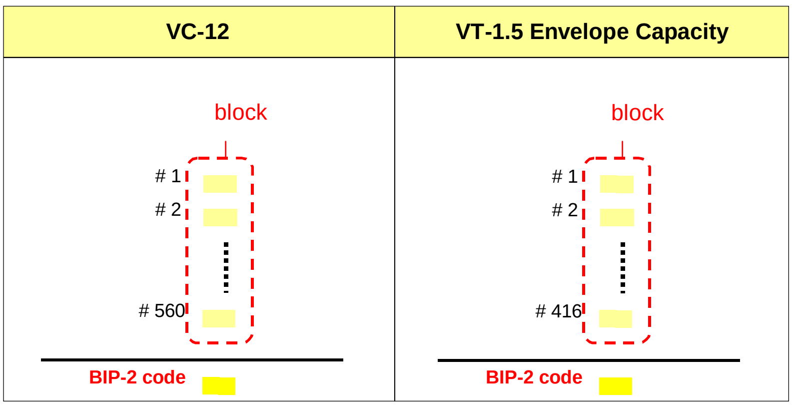
BIP-2		REI	RFI	Signal Label			RDI
1	2	3	4	5	6	7	8

The V5 parity byte monitors the VC-12 (SDH) or the VT-1.5 Envelope Capacity (SONET).



As shown above, a VC-12/VT-1.5 needs 4 SDH/SONET frames to be completely transmitted. So, it takes 500 µs.
The result of the BIP-2 calculation is placed in the following V5 byte. As mentionned previously, the recurrence of the V5 byte is once every 4 SDH/SONET frames.

V5 monitors 140 bytes in SDH (VC-12).
V5 monitors 104 bytes in SONET (VT-1.5 Envelope Capacity).

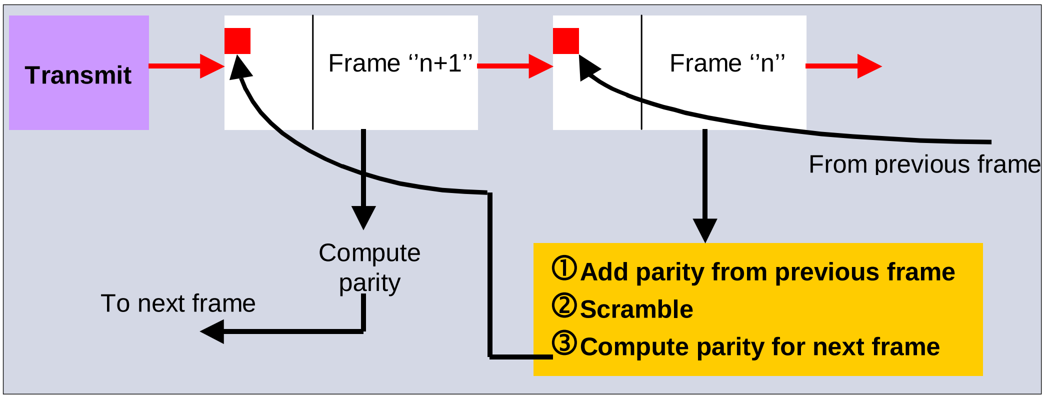


The table below summarizes the V5 parity byte characteristics according to the standard, SDH or SONET:

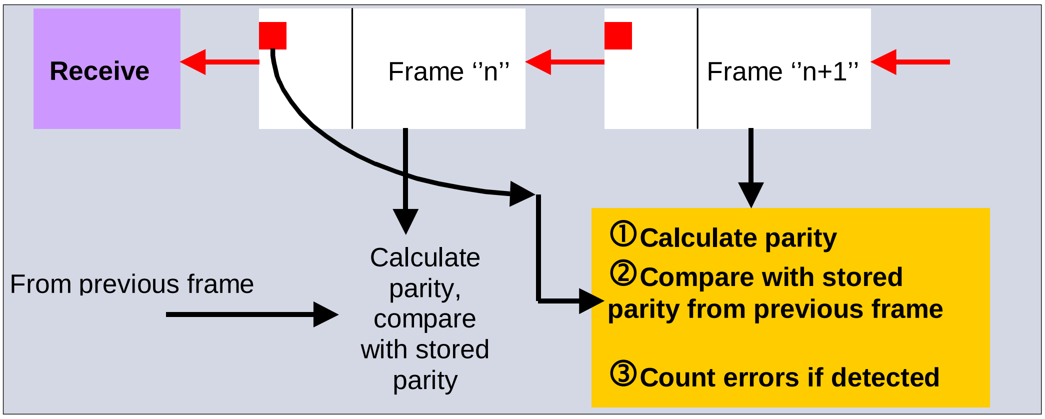
Path	Bit Rate Kbit/s	Bit/block	Block/frame	Block/sec	B3
VC12	2240	1120	1/4	2000	BIP-2
VT-1.5 Envelope Capacity	1664	832	1/4	2000	BIP-2

2.3 BIP Mechanism in SDH/SONET Networks

As mentioned previously, all the BIPs are calculated over their respective portion and the results are placed in the following frame (except for V5 which is inserted every 4 frames).
All the BIPs are calculated prior to scrambling except B1 which is calculated after the frame has been scrambled.
The following example illustrates this specific process with the B1 byte:



Transmitter side (B1 example)



Receiver side (B1 example)

2.4 Maximum Values

Parity bytes monitor blocks. The conceptual definition of a block was introduced in G.826 and remains valid in the current versions of G.826, G.828, G.829 ITU recommendations. All the parity bytes detect errored blocks. And even if there are several errored bits in one block, the parity byte will just detect ONE errored block. This explains why there is a maximum value for B1, B2, B3, V5, which cannot be exceeded.

B1, B2, B3, V5 can be displayed as a rate. The formula is:

$$\text{(B1, B2, B3, V5) rate} = \frac{\text{Number of errored blocks}}{\text{Total number of received blocks}}$$

But it is very usual for SDH/SONET testers to translate this formula in "Equivalent Bit Error Rate (BER)" for practical reasons. This is valid only if there are not too many errors. In concrete terms, if there is no more than one errored bit per block, we can assume that the number of errored bits is equal to the number of errored blocks (and we will see in the next chapters that it is always the case in normal conditions). So, the formula becomes:

$$\text{(B1, B2, B3, V5) Equiv.BER} = \frac{\text{Number of errored blocks } (= \textit{Number of errored bits})}{\text{Number of received blocks * Number of bits / block}}$$

The maximum value for parity byte is reached when all the blocks are errored. The table below gives this maximum Equivalent BER value for each parity byte:

Path	Byte	Bit / Block	Block / Sec	Maximum Equiv. BER
STM64-Reg. OC-192-Sect.	B1	1244160	8000	$8,04\ 10^{-7}$
STM16-Reg. OC-48-Sect.	B1	311040	8000	$3,21\ 10^{-6}$
STM4-Reg. OC-12-Sect.	B1	77760	8000	$1,28\ 10^{-5}$
STM1-Reg. OC-3-Sect.	B1	19440	8000	$5,14\ 10^{-5}$
STM0-Reg. STS1-Sect.	B1	6480	8000	$1,54\ 10^{-4}$
STM64-Mux OC-192-Line	B2	801	12288000	$1,25\ 10^{-3}$
STM16-Mux OC-48-Line	B2	801	3072000	$1,25\ 10^{-3}$
STM4-Mux OC-12-Line	B2	801	768000	$1,25\ 10^{-3}$
STM1-Mux OC-3-Line	B2	801	192000	$1,25\ 10^{-3}$
STM0-Mux STS1-Line	B2	801	64000	$1,25\ 10^{-3}$
VC4-64c STS 192c-SPE	B3	1202688	8000	$8,31\ 10^{-7}$
VC4-16c STS 48c-SPE	B3	300672	8000	$3,32\ 10^{-6}$
VC4-4c STS 12c-SPE	B3	75168	8000	$1,33\ 10^{-5}$
VC4 STS 3c-SPE	B3	18792	8000	$5,32\ 10^{-5}$
VC3 STS 1-SPE	B3	6264	8000	$1,59\ 10^{-4}$
VC-12	V5	1120	2000	$8,92\ 10^{-4}$
VT-1.5 Envelop Capacity	V5	832	2000	$1,20\ 10^{-3}$

In conclusion:

B1: The maximum number of errors that B1 can detect is reduced with an increase in the line rate. This is because the number of parity bits remains the same while the size of the block increases.

B2: The maximum number of errors that B2 can detect remains constant with an increase in the line rate. This is because the quantity of parity bits increases in the same proportion as the number of blocks.

B3: The maximum number of errors that B3 can detect remains constant with an increase in line rate, but it is dependent on the mapping type. B3 is the path-error monitoring function associated with the payload.

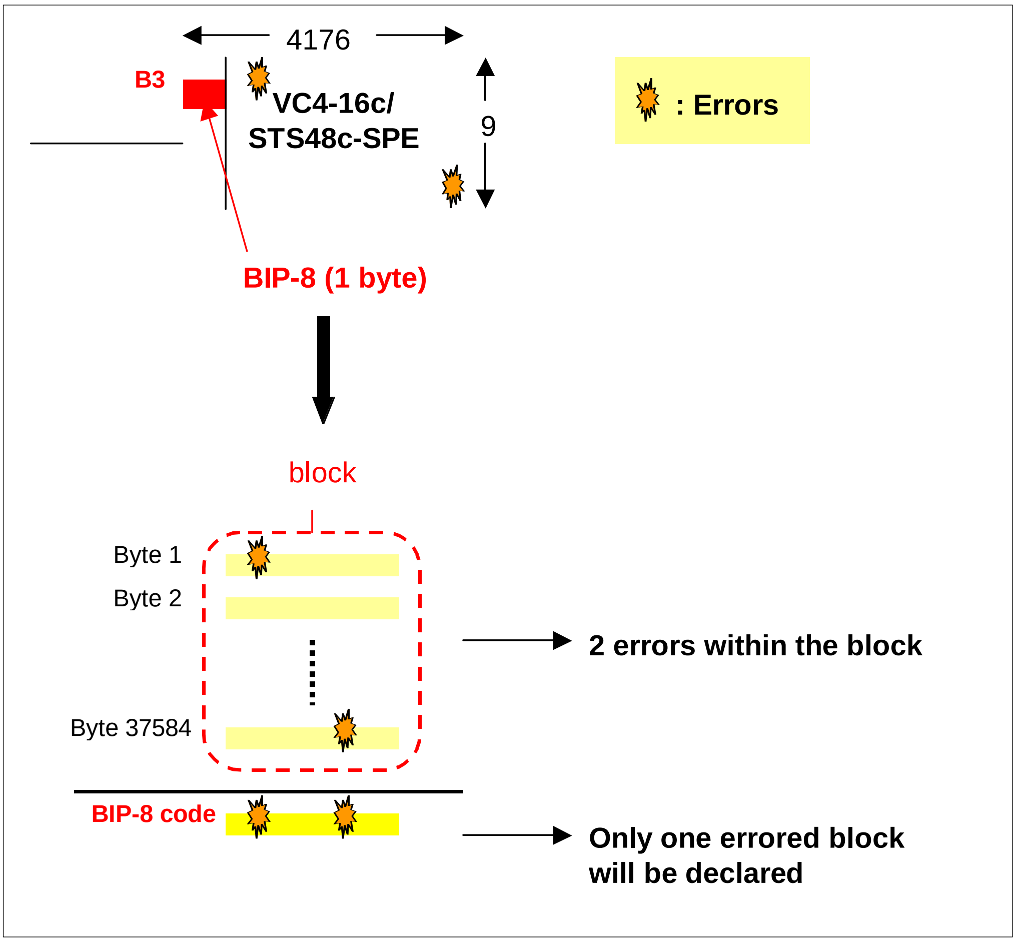
3.0 BIP: Limitations

BIP calculation methods have some limitations. In particular cases, all the errors occuring during the transmission of the SDH/SONET frames may not be detected.
These particular cases are described below:

3.1 Errors occuring within the Same Block

As already mentioned, each parity byte monitors a block. Even if there are several errored bits within the same block, only one errored block will be detected.

The next example shows what happens with the B3 byte when several errors occur in the VC4-16c/STS 48c-SPE of an STM16/OC-48 frame.



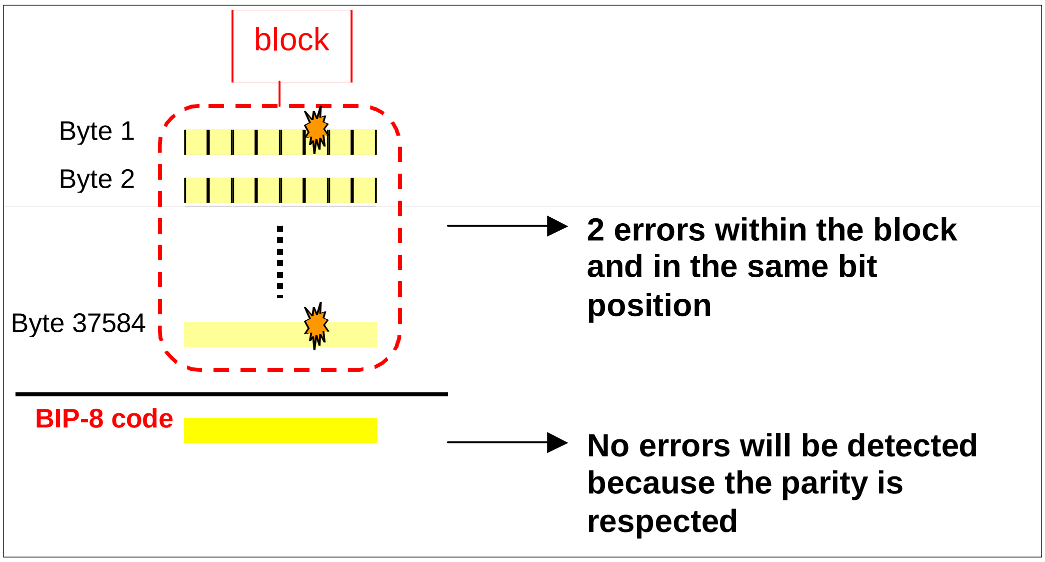
In short, on the reception side, there is no difference between:

3.2 Errors occuring at the Same Relative Bit Position

Another special case may appear, which is in fact an exceptional example of the case described in the previous paragraph: "error occur within the same block AND at the same relative bit position".

In this case, if the number of errors is even, then these errors will not be detected because the parity is respected.

For example:

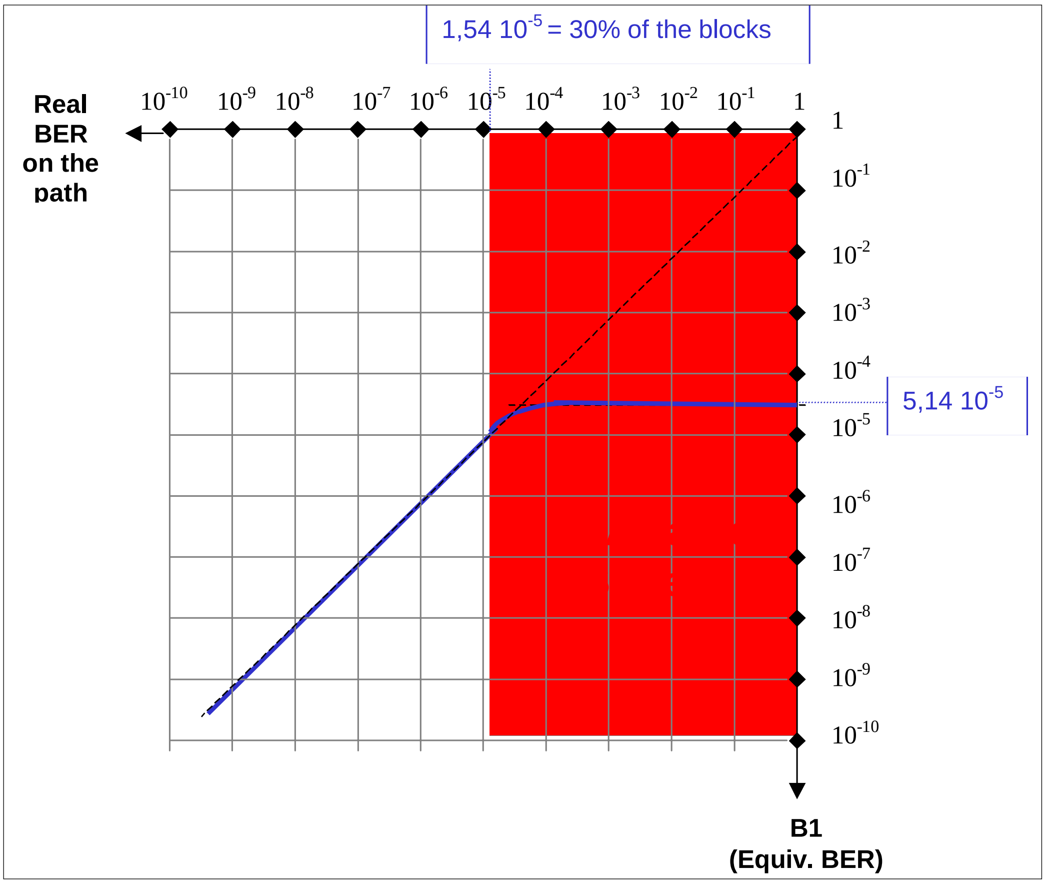


The probability of errors occuring within the same block (and occasionally in the same bit position) is very low in normal conditions [1].
The higher the number of errors, the higher the probability of meeting the special cases described above.
But in practice, when there is a high bit error rate, the corresponding path is declared in unavailability state and the errors are no longer cumulated.

The graph below shows the limitations of BIP and the "unavailable state" area with the B1 parity byte of an STM1/OC-3 frame:

Notes:

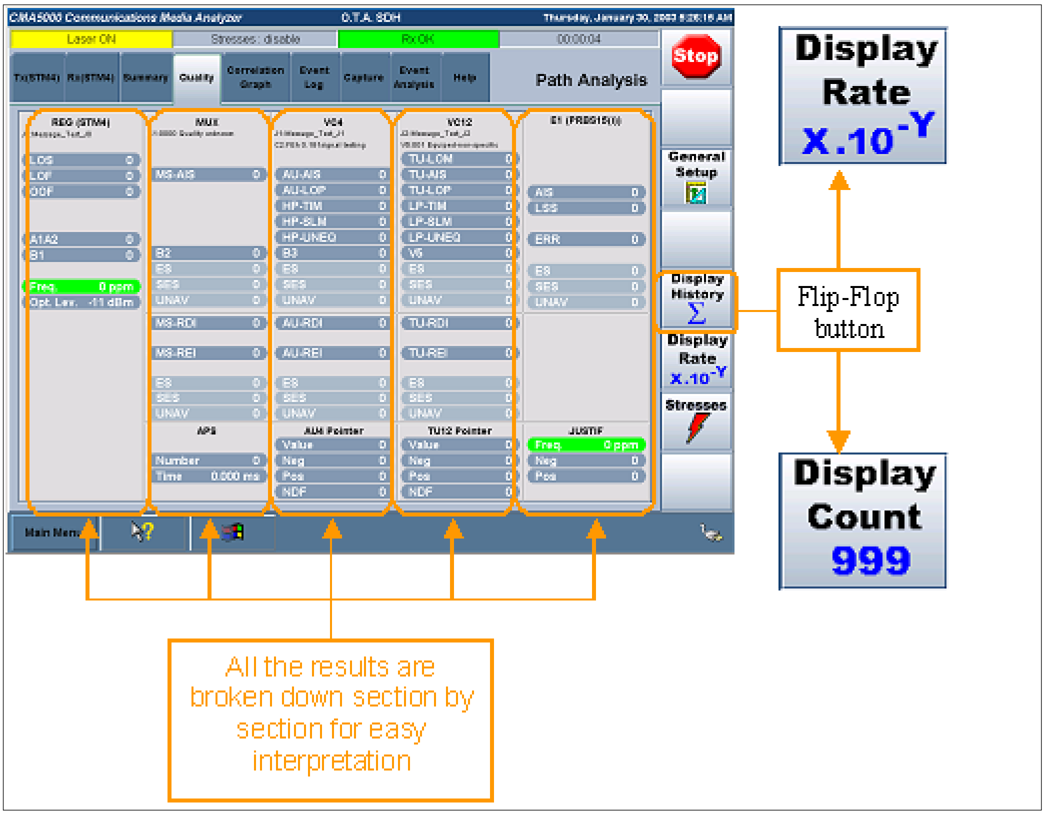
[1] All recommendations give the same definition of unavailable time: an unavailable period starts with the occurence of the first SES of 10 consecutive Severly Errored Second (SES). In G.826, G.828, an SES event is declared when at least 30% of the received blocks in a second are errored.



4.0 Practical Example with OTA Application

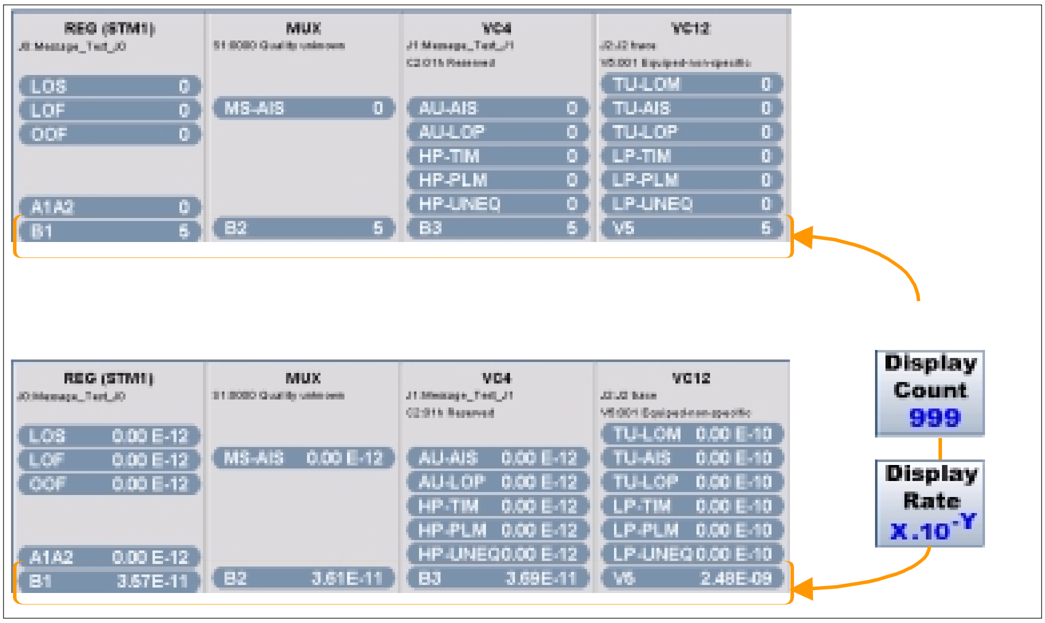
The “Optical Transport Analysis” (OTA) application of the NetTest CMA 5000 platform provides a very easy way to display the parity bytes as a rate.

The “Quality” window (accessed via the “Quality” tab) shows all the analyzed parameters in a single window and a flip-flop button allows the user to select the display mode for the results (Count or Rate mode):

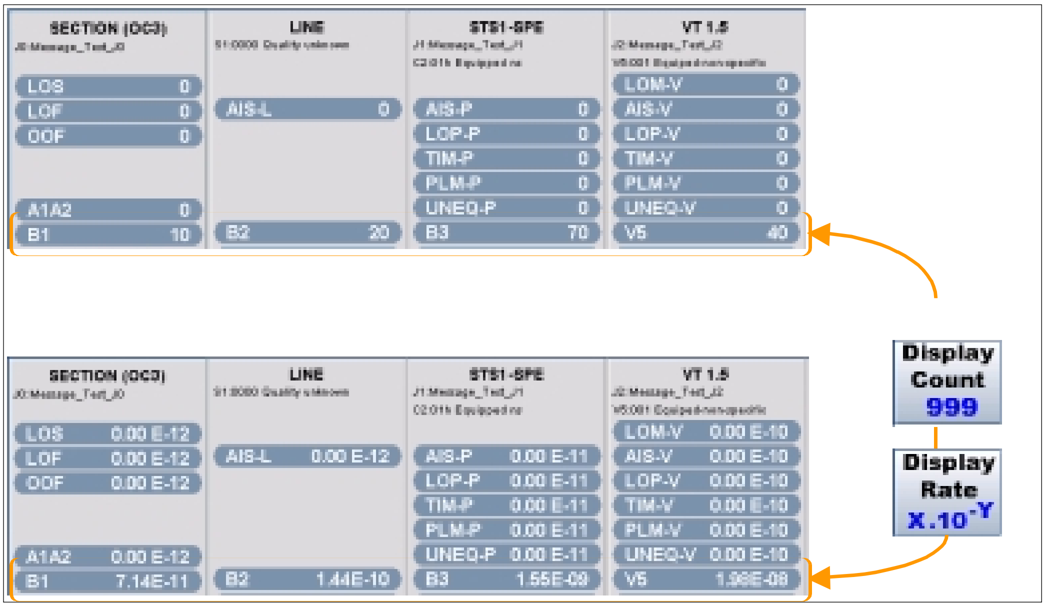


Examples:

STM1 measurement after 15 minutes:



OC-3 measurement after 15 minutes:



5.0 Bibliography

Standards	
IUT-T	G.707: Network Node Interface for the SDH Annex D: Byte structure and frame layout for the VC-4 and VC-3 containers Annex E: Byte structure and frame layout for the VC-2, VC-11 and VC-12 containers
	G.783: Principal characteristics of multiplexing equipment for the synchronous digital hierarchy
	G.826: Error performance parameters and objectives for international, constant bit rate digital paths at or above the primary rate
	G.828: Defines parameters and objectives for SDH paths
Bellcore	GR-253: SONET Transport System: Common Generic Criteria
ANSI	T1.105 - 1995: SONET - Basic description including multiplex structure, rates and formats T1.105.02: SONET - Payload mapping

Technical Paper
• NetTest technical paper: "Availability and Performance Evaluation of your PDH/SDH Networks" - Ref: TXP-C-4006 Ed.1

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